

What is claimed is:

1 1. A computer system, unaffected by memory module
2 instability, comprising:

3 at least one memory mirror unit controlling a
4 plurality of memory modules and receiving an
5 error control signal, wherein each of the
6 memory mirror units writes data to the
7 corresponding memory modules during a write
8 cycle and activates a first memory module among
9 the memory modules, reading data during a read
10 cycle;

11 a memory controller enabling the error control
12 signal upon detection of a read error in the
13 first memory module, wherein the memory mirror
14 unit disables the first memory module and
15 activates a second memory module among the
16 memory modules when the read error occurs in
17 the first memory module.

1 2. The computer system as claimed in claim 1,
2 further comprising:

3 a central processing unit (CPU); and

4 a system interruption device providing an
5 interruption signal to the CPU to interrupt
6 system operations and then activate the
7 corresponding error control signal when the
8 memory controller detects the read error.

1 3. The computer system as claimed in claim 2,
2 wherein each memory mirror unit receives a corresponding

3 error control signal for control of corresponding memory
4 modules.

1 4. The computer system as claimed in claim 3,
2 wherein the memory controller determines that the read
3 error has occurred when the memory controller detects an
4 irreparable error in the first memory module of
5 corresponding memory modules during the read cycle.

1 5. The computer system as claimed in claim 3,
2 wherein the memory controller determines that the read
3 error has occurred when the memory controller detects
4 that the number of errors in the first memory module
5 reaches a predetermined value.

1 6. The computer system as claimed in claim 3,
2 wherein each memory mirror unit controls only a first and
3 second memory module, each memory mirror unit activating
4 the first and second memory modules during the write
5 cycle and only activating the first memory module during
6 the read cycle, and wherein the memory controller
7 activates the error control signal and the memory mirror
8 unit only activates the second memory module upon
9 detection of the read error in the first memory module
10 during the read cycle.

1 7. The computer system as claimed in claim 3,
2 wherein each memory mirror unit comprises:

3 a first AND gate comprising a first input terminal,
4 a second input terminal, a third input terminal
5 receiving a row selecting signal, a fourth
6 input terminal, a fifth input terminal

receiving a write enable signal, and a sixth
input terminal receiving the error control
signal;

a first inverter comprising an input terminal
receiving a chip control signal and an output
terminal coupled to the first input terminal of
the first AND gate;

a second inverter comprising an input terminal
receiving a first enable signal and an output
terminal coupled to the second input terminal
of the first AND gate;

a third inverter comprising an input terminal
receiving a column selecting signal and having
an output terminal coupled to the fourth input
terminal of the first AND gate;

a second AND gate comprising a first input terminal,
a second input terminal, a third input terminal
receiving the row selecting signal, a fourth
input terminal, a fifth input terminal
receiving the write enable signal, and a sixth
input terminal;

a fourth inverter comprising an input terminal
receiving the chip control signal and an output
terminal coupled to the first input terminal of
the second AND gate;

a fifth inverter comprising an input terminal
receiving a second enable signal and an output
terminal coupled to the second input terminal
of the second AND gate;

a sixth inverter comprising an input terminal receiving the column selecting signal and an output terminal coupled to the fourth input terminal of the second AND gate;

a seventh inverter comprising an input terminal receiving the error control signal and an output terminal coupled to the sixth input terminal of the second AND gate;

a first switch comprising an output terminal, a control terminal, and an input terminal receiving the first enable signal;

a second switch comprising an input terminal receiving the second enable signal, an output terminal coupled to the output terminal of the first switch and a control terminal receiving the chip enable signal;

an eighth inverter comprising an input terminal receiving the chip enable signal and an output terminal coupled to the control terminal of the first switch;

a first OR gate comprising a first input terminal receiving the first enable signal, a second input terminal coupled to the output terminal of the first AND gate, and an output terminal coupled to the first memory module; and

a second OR gate having a first input terminal coupled to the output terminal of the first switch, a second input terminal coupled to the output terminal of the second AND gate, and an

65 output terminal coupled to the second memory
66 module.

1 8. The computer system as claimed in claim 7,
2 wherein the chip control signal equalizes the addresses
3 of the first and second memory modules.

1 9. The computer system as claimed in claim 7,
2 wherein the memory controller determines that a read
3 error has occurred when the memory controller detects an
4 irreparable error in the first memory module during the
5 read cycle.

1 10. The computer system as claimed in claim 8,
2 wherein the memory controller determines that a read
3 error has occurred when the memory controller detects the
4 number of errors in the first memory module during the
5 read cycle reaching a predetermined value.

1 11. The computer system as claimed in claim 9,
2 wherein the chip control signal and the error control
3 signals are output from a general input/output device of
4 the computer system and wherein the first enable signal,
5 the second enable signal, the row selecting signal, and
6 the column selecting signal are output from the memory
7 controller.

1 12. The computer system as claimed in claim 9,
2 wherein the chip control signal is output from a general
3 input/output device of the computer system and wherein
4 the error control signal, the first enable signal, the
5 second enable signal, the row selecting signal, and the

6 column selecting signal are output from the memory
7 controller.

1 13. The computer system as claimed in claim 10,
2 wherein the error control signal is output from a general
3 input/output device of the computer system and wherein
4 the first enable signal, the second enable signal, the
5 row selecting signal, and the column selecting signal are
6 output from the memory controller.

1 14. The computer system as claimed in claim 10,
2 wherein the chip control signal is output from a
3 represent general input/output device of the computer
4 system and wherein the error control signal, the first
5 enable signal, the second enable signal, the row
6 selecting signal, and the column selecting signal are
7 output from the memory controller.

1 15. A method for controlling memory of a computer
2 system, the method comprising the steps of:

3 providing at least one memory mirror unit, each
4 controlling a memory module group having a
5 plurality of memory modules;

6 equalizing addresses of the memory modules inside
7 each memory module group;

8 writing data to the corresponding memory modules
9 according to a write address during a write
10 cycle; and

11 reading a first memory module according to a read
12 address during a read cycle;

13 wherein the computer system activates an error
14 control signal received by the corresponding
15 memory mirror unit to select a second memory
16 module from corresponding memory modules when a
17 read error occurs in the first memory module.

1 16. The method as claimed in claim 15, wherein the
2 computer system determines that the read error has
3 occurred when an irreparable error occurs in the first
4 memory module of the corresponding memory modules.

1 17. The method as claimed in Claim 15, wherein the
2 computer system determines that the read error has
3 occurred when the number of errors in the first memory
4 module reaching a predetermined value.

1 18. A method for controlling memory of a computer
2 system, the method comprising the steps of:
3 providing at least one the memory mirror unit each
4 controlling a first and second memory module;
5 equalizing addresses of the first and second memory
6 modules;
7 writing data to first and second memory modules
8 according to a write address during a write
9 cycle; and
10 reading the corresponding first memory module
11 according to a read address reading data during
12 a read cycle;

14 wherein the computer system activates an error
15 control signal received by the corresponding

16 memory mirror unit to select a corresponding
17 second memory module when a read error in the
18 corresponding first memory module is detected.

1 19. The method as claimed in claim 18, wherein the
2 computer system determines that the read error has
3 occurred when an irreparable error occurs in the first
4 memory module during the read cycle.

1 20. The method as claimed in Claim 18, wherein the
2 computer system determines that the read error has
3 occurred when the number of errors in the first memory
4 module reaches a predetermined value.